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8E4015

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B. Tech. (Sem. VIII) (Main/Back) Examination, April/May-2011
Computer
8CS2 CAD FOR VLSI Design

Time : **3** Hours] [Total Marks : **80**
[Min. Passing Marks : **24**

*Attempt any **five questions**, selecting **one question** from **each unit**. **All** questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly, Units of quantities used/calculated must be stated clearly.*

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. Nil 2. Nil

UNIT – I

1 (a) Describe two factors that make CAD tools necessary for VLSI Design. What type of specifications needed for CAD tools ? **6**

(b) Write design flow for processing structural description of circuits on platform containing more than one FPGA. Explain each step in brief. **10**

OR

(a) Describe diversity of applications in the context of modern digital systems. **6**

(b) Explain CAD flow for ASIC that take care of multiple views and design entry at different stages. **10**

UNIT – II

2 (a) Describe the characteristics that distinguish Hardware description language from software language.

6

(b) Giving example distinguish between :

(i) Concurrent and Sequential assignment.

(ii) Inertial and transport delay.

10

OR

(a) List all the translations in the following using delta delay concept of VHDL.

```
ARCHITECTURE concurrent OF timing_demo IS
SIGNAL a, b, c : BIT : = '0';
BEGIN
    a < = '1';
    b < = NOT a;
    c < = NOT b;
END concurrent;
```

6

(b) Explain the following VHDL requirements :

(i) Generic Design

(ii) Timing Control

(iii) Support for Design Hierarchy

(iv) Library Support

10

UNIT – III

3 (a) Explain Physical and enumeration type data in VHDL.

6

(b) Write a VHDL program for behavioral single bit comparator. What are the components needed for structural one bit-comparator.

10

OR

(a) Explain binding alternatives in VHDL.

6

(b) What is test bench in VHDL ? Write a program for test bench of 4-to-1 multiplexor.

10

UNIT – IV

4 (a) Explain the following attributes of a signal
EVENT, LAST_EVENT, LAST_VALUE, TRANSACTION

6

(b) Explain the concept of overloading in VHDL. Write a program that explains the concept of overloading.

10

OR

(a) Distinguish between pre-defined and user-defined attributes. Giving example explain one user defined attribute.

6

(b) Explain the following array attributes.
RANGE, REVERSE_RANGE, LOW, RIGHT, LENGTH
Write VHDL program that uses atleast two array attributes.

10

UNIT – V

5 (a) What is the use of Synthetic Circuits ? How are these circuits different than Real Circuits ?

6

(b) Write two or more parameters used in generating Synthetic Circuits. Explain Synthetic Circuit generation process.

10

OR

(a) Name three repositories that provide circuits. Write information supplied by repositories related to circuits.

6

(b) What is state machine synthesis ? Write a program in VHDL using state machine synthesis for a sequence detector that detects '1011'.

10